REMARKS

Election/Restrictions – Examiner Interview Summary

A provisional restriction requirement was made on June 21, 2004 during a telephonic interview between Applicant's attorney and the Examiner.

Applicant hereby affirms the election of group I (claims 1-30). The Applicant cancels groups II (claims 31-44 and 49-52), group III (claims 45-48) and group IV (claims 53-56) without prejudice and reserves the right to reintroduce the claims in divisional applications at a later date.

In the Drawings

New formal drawings are enclosed per the Examiners request. Drawings enclosed do not represent new subject matter.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-30 were rejected under 35 U.S.C. §103(a) as being unpatenable over Nozoe et al. (U.S. Patent No. 6,351,412). Applicant respectfully traverses this rejection and feels that claims 1-30 are allowable for the following reasons.

The Examiner stated, in part, that Nozoe et al. disclosed a non-volatile memory device having an error correction function capable of outputting uncorrected read-out data while simultaneously generating syndromes (*See*, Office Action mailed on July 2, 2004, Page 5). The Examiner also stated that the non-volatile memory device of Nozoe et al. disclosed a non-volatile memory array with spare memory sections and a defective address register that allowed defective bits of the memory array to be replaced and addressing redirected to the spare memory section (*See*, Office Action mailed on July 2, 2004, Pages 5 and 8). The Examiner further stated that it would have been obvious to one skilled in the art to incorporate a state machine in the non-volatile memory device of Nozoe et al. to execute the algorithms as the Applicants claimed invention does (*See*, Office Action mailed on July 2, 2004, Pages 8-9).

The Applicant disagrees and maintains that Nozoe et al. discloses a non-volatile memory device that, to increase the speed of read access, outputs the uncorrected data read from the memory array while error correction code (ECC) stored with the data is processed to check for

data errors (generate syndromes). If an error is detected, the memory device of Nozoe et al. indicates the error and allows the system to re-read the corrected data if it is so desired.

The Applicant respectfully maintains that Nozoe et al., in disclosing the spare memory sections and a defective address register that allowed defective bits of the memory array to be replaced, does not disclose or suggest storing data on the type of defect in the address location it is replacing as claimed in the Present Application; it only teaches replacing the location with a spare/redundant memory location and storing the address of replaced location to allow future accesses to be redirected to the replacement. *See, e.g.*, Nozoe et al., column 10, lines 32-37. The Applicant also notes that an ECC code and ECC checking circuitry are used to error check the data the ECC code is stored with in the memory array and allows for selective error detection and correction and would be recognized as such by one skilled in the art. The Applicant therefore asserts that the ECC codes and ECC circuitry are not related to the defective address location register or address redirection circuitry and does not redirect the memory read access to a different location and does not store error data or type of error, as seems to be asserted by the Examiner. *See, e.g.*, Nozoe et al., column 1, line 62 to column 2, line 2, column 2, lines 33-67, and column 10, lines 32-37.

Applicant therefore respectfully submits that Nozoe et al. does not teach or suggest a non-volatile memory device with a memory array having primary and redundant memory cells, where redundant fuse circuitry of the memory device is used to replace the primary memory cells with the redundant memory cells and the redundant fuse circuitry stores an error code indicating a type of defect in the primary memory cells in addition to the address of the defective primary memory cells in the array, as maintained by the Examiner.

In addition to the above arguments, the Applicant further contends that there is no motivation or suggestion to modify the reference in this manner. Specifically, Applicant contends that to modify Nozoe et al. to provide storage of defect types would require a modification of Nozoe et al.'s defective address register to allow storage of defect type as well as the defect address location. Nozoe et al. expressly teaches away from this and only states that the "defect register retains a location (address) of a defective bit." As stated above, as ECC codes and ECC circuitry are not related to the defective address location register or defective address redirection circuitry and do not redirect the memory read access to a different location or store error data or type of error, the ECC codes of Nozoe et al. are restricted to data error correction of read-out data and not memory array defect replacement. *See, e.g.*, Nozoe et al., column 1, lines 54-59, column 4, lines 24-42, and column 10, lines 32-37. Applicant also finds

no motivation or suggestion to modify the operation of Nozoe et al. expressly or impliedly contained in the Nozoe et al. reference, and the Office Action does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. Applicant thus submits that the Office has also failed to meet its burden of establishing a *prima facie* case of obviousness. *See* MPEP § 706.02(j) ("The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'").

Applicant's claim 1 recites, in part, "redundant fuse circuitry used to replace the primary memory cells with the redundant memory cells, wherein the redundant fuse circuitry stores an error code indicating a type of defect." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having redundant fuse circuitry used to replace the primary memory cells with the redundant memory cells, wherein the redundant fuse circuitry stores an error code indicating a type of defect. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 1.

Applicant's claim 8 recites, in part, "at least one register to store an address of a defective element in a primary memory array, the register having at least one data bit to store an error code." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having at least one register to store an address of a defective element in a primary memory array, the register having at least one data bit to store an error code. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 8.

Applicant's claim 12 recites, in part, "a register for each redundant array element to store an address of a defective element in the memory array, each register further stores an error code." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having a register for each redundant array element to store an address of a defective element in the memory array, each register further stores an error code. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 12.

Applicant's claim 17 recites, in part, "a register for each redundant row to store the address of the associated defective row, each register further stores an error code, wherein the error code indicates the type of error the redundant row is used to correct." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having a

register for each redundant row to store the address of the associated defective row, each register further stores an error code, wherein the error code indicates the type of error the redundant row is used to correct. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 17.

Applicant's claim 20 recites, in part, "a register for each redundant column to store the address of the associated defective column, each register having at least one extra bit to store an error code, wherein the error code indicates the type of error in the at least one defective column." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having a register for each redundant column to store the address of the associated defective column, each register having at least one extra bit to store an error code, wherein the error code indicates the type of error in the at least one defective column. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 20.

Applicant's claim 24 recites, in part, "a register for each redundant row to store the address of an associated defective row, each register further having at least one bit to store an error code, wherein the error code indicates the type of defect in the associated defective row." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having a register for each redundant row to store the address of an associated defective row, each register further having at least one bit to store an error code, wherein the error code indicates the type of defect in the associated defective row. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 24.

Applicant's claim 28 recites, in part, "a register for each redundant row and each redundant column to store the addresses of associated defective rows and columns, each register having at least one bit to store an error code, wherein the error code indicates the type of defect the redundant row or column is used to correct." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having a register for each redundant row and each redundant column to store the addresses of associated defective rows and columns, each register having at least one bit to store an error code, wherein the error code indicates the type of defect the redundant row or column is used to correct. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 28.

Applicant respectfully contends that the Examiner has not met the burden of establishing a *prima facie* case of obviousness in regards to claims 1, 8, 12, 17, 20, 24 and 28, and, in addition, that claims 1, 8, 12, 17, 20, 24 and 28 as pending have been shown to be patentably distinct from the cited reference, either alone or in combination with the Examiner's taking of

official notice. As claims 2-7, 9-11, 13-16, 18-19, 21-23, 25-27 and 29-30 depend from and further define claims 1, 8, 12, 17, 20, 24 and 28, respectively, they are also believed to be allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-30.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 9/13/04

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